About 250/285 GHz push–push oscillator using differential gate equalisation in digital 65-nm CMOS

Bassem Fahs, Kefei Wu, Walid Aouimeur, Muhammad Waleed Mansha, Christophe Gaquière, Patrice Gamand, Wojciech Knap, Mona M. Hella

About 250/285 GHz push–push oscillator using differential gate equalisation in digital 65-nm CMOS

Bassem Fahs[1] ✉, Kefei Wu[1], Walid Aouimeur[2], Muhammad Waleed Mansha[1], Christophe Gaquière[2], Patrice Gamand[3], Wojciech Knap[4], Mona M. Hella[1]

[1]*Department of Electrical, Computer and Systems Engineering, Rensselaer Polytechnic Institute, Troy, NY 12180, USA*
[2]*Institut d'Electronique de Microélectronique et de Nanotechnologie (IEMN), University of Lille, 59652 Villeneuve d'Ascq, France*
[3]*XLIM Laboratory, Labex SIGMA-LIM, University of Limoges, 123 Avenue A. Thomas, 87060 Limoges, France*
[4]*International Research Laboratory CENTERA, Institute of High Pressure Physics, Polish Academy of Sciences, 01-142 Warsaw, Poland*
✉ *E-mail: fahsb@rpi.edu*

Abstract: This study presents a push–push oscillator architecture based on differential gate equalisation to enhance the oscillation frequency while providing relatively high output power with ultra-compact layout form factor. The frequency enhancement is derived as a function of the equivalent RLC model of the oscillator's main constituents. The proposed principle is applied to a terahertz oscillator in the 200–300 GHz range to mitigate the excessive substrate and skin effect losses in standard digital 65-nm complementary metal–oxide–semiconductor technology at such high frequencies. The design concept is validated using two single-stage push–push oscillators. The first oscillator shows −8.1 dBm output power at 250 GHz oscillation frequency and −106.8 dBc/Hz phase noise at 10 MHz offset while consuming 76 mW power from 1.5 V DC supply voltage. The chip area is 200 × 250 μm^2. The second oscillator provides −14.8 dBm output power at 285 GHz and −106 dBc/Hz phase noise at 10 MHz offset with 80 mW power consumption from 1.5 V DC supply. The chip area is 200 × 200 μm^2.

1 Introduction

The unique properties for the electromagnetic (EM) waves in the terahertz and sub-mmWave frequency ranges (penetration, absorption, scattering etc.) promise disruptive technological advances in short-distance high data-rate communication, spectroscopy, bio-medical diagnosis, imaging and others. Existing THz systems are mostly bulky, expensive and based on photonic realisations [1]. Integrated systems using low-cost standard integrated circuit (IC) technologies have become a requirement to provide compact, portable, cost-effective and adaptive commercial solutions [2]. It remains that most of the used standard IC processes [complementary metal–oxide–semiconductor (CMOS) or bipolar] have their own frequency limitations and increased parasitic losses at such high frequencies, which seriously reduce the output transmission power and impede the THz solutions from moving towards low-cost commercial products.

One approach of generating power at THz frequencies is based on amplifier–multiplier chains with the input taken from a stable low-frequency source to generate the output signal by mixing effects at higher harmonic frequencies as in [3–6]. This approach suffers from high DC power and large chip area. In addition, the phase noise of the output is a function of the input signal's phase noise and thus a stable input frequency source is required. Another approach for THz signal generation is direct generation using high-frequency coupled oscillators to extract the higher order harmonics of the fundamental oscillation frequency. A small chip size could be achieved with low DC power and the signal source in this case is self-contained. Push–push [7–9] and self-feeding harmonic [10] oscillators use balanced structures and symmetric layouts to extract the second harmonic. Triple-push [11–13] and quad-push [14] oscillator topologies have also been utilised to achieve higher oscillation frequencies at the third and fourth harmonics, respectively. However, triple-push oscillators suffer from complexity in generating a symmetric layout while the output power of the fourth harmonic in the case of quad-push oscillators is relatively small. To increase the output power, either multiple core oscillators are coupled [13] or arranged in an array format [15].

In THz and sub-mmWave frequency ranges, substrate losses and skin effects decrease the quality factor of passive devices and varactors making it more challenging to extract the highest power from the transistors within the oscillator while targeting a small layout form factor. This is particularly true for digital CMOS processes which tend to have a thin back end of line. Design examples proposed in the literature include using a slow-wave coplanar waveguide (CPW) which has lower loss than a standard or grounded CPW to implement the tank [13]. Varactor-based techniques are applied using hyper-abrupt junction varactor to increase the linearity of C–V characteristics or the parasitic capacitance of metal–oxide–semiconductor (MOS) transistor in [16, 17], respectively, with both oscillators operated in the 100 GHz band.

In this paper, a push–push oscillator architecture based on a differential structure is demonstrated. The proposed approach is capable of achieving a compact form factor through a simplified routing with less parasitics in addition to reduced DC power consumption. We show that the use of differential equalisation between the cross-coupled metal–oxide–semiconductor field-effect transistor gates reduces the equivalent capacitance at the gate level which results in increasing the frequency of oscillation. A frequency enhancement factor (FEF) is derived as a function of the equivalent RLC model of the oscillator design parts. The design is validated using two single-stage push–push oscillators implemented in 65 nm standard digital CMOS technology. The first oscillator shows −8.1 dBm output power at 250 GHz oscillation frequency while consuming 76 mW power from 1.5 V DC supply with 200 × 250 μm^2 chip area. The second oscillator gives −14.8 dBm output power at 285 GHz with 80 mW power from 1.5 V DC supply and 200 × 200 μm^2 chip area.

The paper is organised as follows. In Section 2, the general push–push design principle with differential gate equalisation is presented. In Section 3, the implementation and the different oscillator parts modelling are detailed. Section 4 gives the experimental setup description and the measurement results. Finally, conclusions are drawn in Section 5.

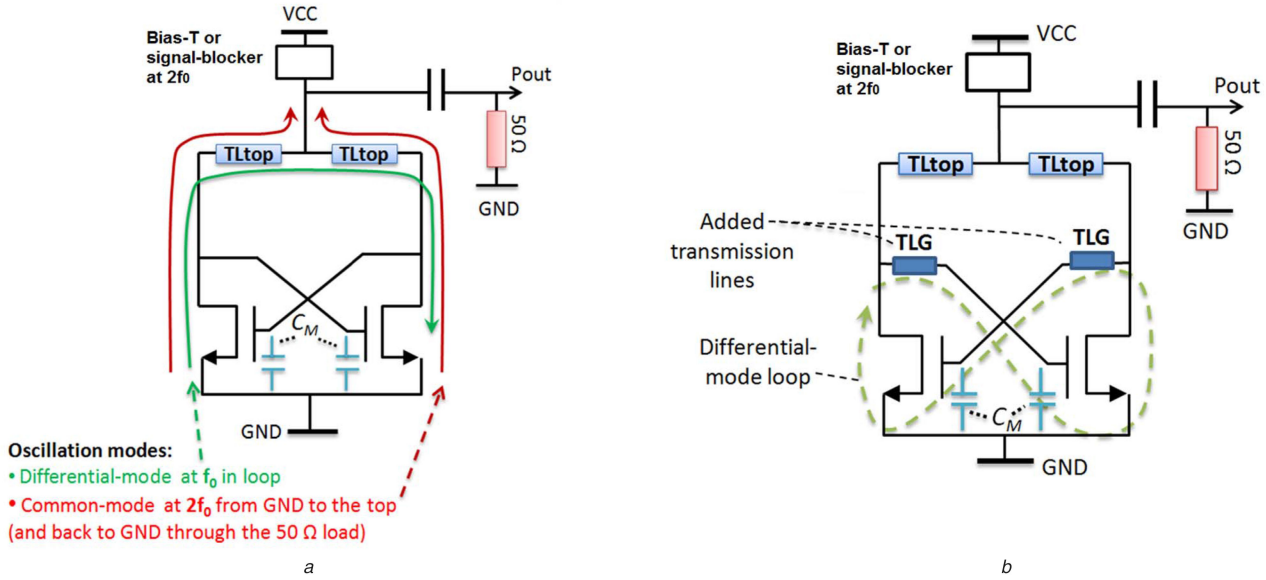


Fig. 1 *Push–push oscillator*
(a) With a traditional cross-coupled active gm-core,
(b) With added TLG

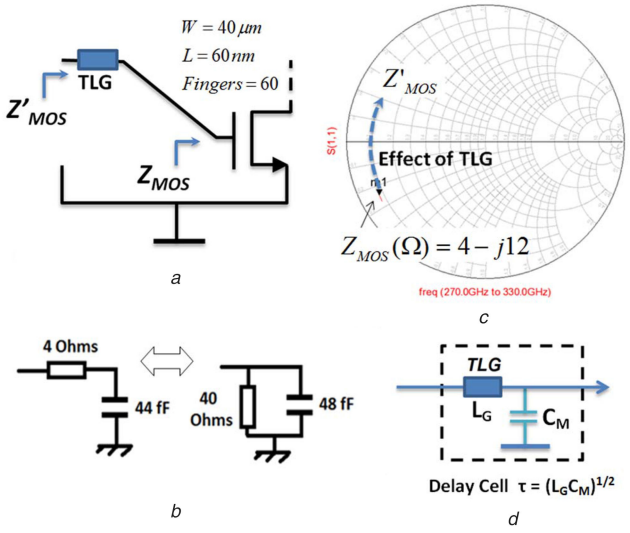


Fig. 2 *MOS characteristics shown through*
(a) The gate impedance at 300 GHz represented by Z_{MOS} and Z'_{MOS} after TLG,
(b) Equivalent Z_{MOS} model with series and parallel elements,
(c) Effect of the added transmission line (TLG) on transforming the equivalent MOS capacitive impedance (Z_{MOS}) to an inductive impedance (Z'_{MOS}),
(d) Delay cell formed by TLG and the equivalent MOS capacitance (C_M)

2 Design principle

A typical oscillator architecture is based on the use of a resonating part and a transconductance gm-core providing the negative resistance to compensate for the tank losses. Fig. 1*a* shows a differential oscillation mode at a frequency f_0, where the signal goes through an internal loop without the need to be referenced to the ground (GND). The push–push behaviour can be described as the circulation of the common-mode (CM) signal at a frequency $2f_0$ (or generally at even harmonics of f_0) through a loop going from GND to the output load and back to GND. The output signal could be either electrical or radiated (output terminated with an antenna). In the case of an electrical signal, a bias-T or a signal blocker at $2f_0$ could be used to provide the DC supply voltage (VCC). Transmission lines (TL) use at the intended frequency range is preferred as they present much lower losses than lumped elements, inductor and capacitor-based tanks [18].

To increase the output power from the oscillator, the conversion from differential mode to CM signal should be optimised. Since part of the CM power at even harmonics (mainly at $2f_0$) travelling through the gm-core from GND to the top load will be absorbed by the gm-core transistors' gates, this reduces the power delivered to the output. Adding a 'signal blocking' impedance or transmission line before the gates can prevent such losses if the realised impedance transformation goes from capacitive to inductive. This can also be expressed as a function of gate-blocking TL (TLG) parameters, i.e. the characteristic impedance $Z_{0,TLG}$ and the electrical length φ_{TLG} to maximise the CM power transfer to the output at $2f_0$, as was also reported in [10]. Different ($Z_{0,TLG}$, φ_{TLG}) can be determined through simulations to satisfy the maximum output power condition. In this paper, the goal is to build on this understanding and also realise a compact layout with short TLG to minimise the associated losses with the series resistance. On the top side, the TLtop transmission lines depicted in Fig. 1*b* also contribute to the differential-mode circulation. However, they do not influence the frequency enhancement effect which will be introduced later. Further considerations for TLtop sizing are presented in the implementation section.

Based on the previous discussion, a TLG is added to the cross-coupled oscillator structure, as shown in Fig. 1*b*. The used MOS transistor (MOST) size is selected to get maximum transition frequency (f_T) performance. With $f_T = g_m/2\pi C_{in}$, where g_m is the MOS transconductance and C_{in} is its input gate capacitance, f_T allows selecting optimum MOST size and bias point settings regardless of the input/output loading conditions. The MOS size was accordingly set to a width of 40 µm, a gate length of 60 nm and folded into 60 fingers. The gate impedance characterisation, represented by Z_{MOS} in Figs. 2*a–c*, gives $Z_{MOS} = 4 - j12$ at 300 GHz, which can be modelled by an equivalent capacitance $C_M \simeq$ 48 fF. The effect of TLG can hardly render infinite input impedance from the gate level. However, making the transformed impedance (Z'_{MOS}) inductive would relax the CM impedance matching. Setting TLG to an electrical length of roughly 30° and 50-Ω characteristic impedance is equivalent to a series inductance of $L_G \simeq 15$ pH. Considering either TLG or L_G would sensitively give the same impedance rotation starting from Z_{MOS} on the Smith chart shown in Fig. 2*c*. This also means that the parasitic capacitance for TLG, i.e. $C_G \simeq 6$ fF (calculated with $Z_c = (L_G/C_G)^{1/2} = 50\ \Omega$) can be neglected with respect to C_M. The path through TLG to the MOST can thus be considered as a delay cell formed basically by L_G and C_M.

The oscillation frequency (f_0) is dictated by two parallel paths. The first path is through TLtop and the second one is through the

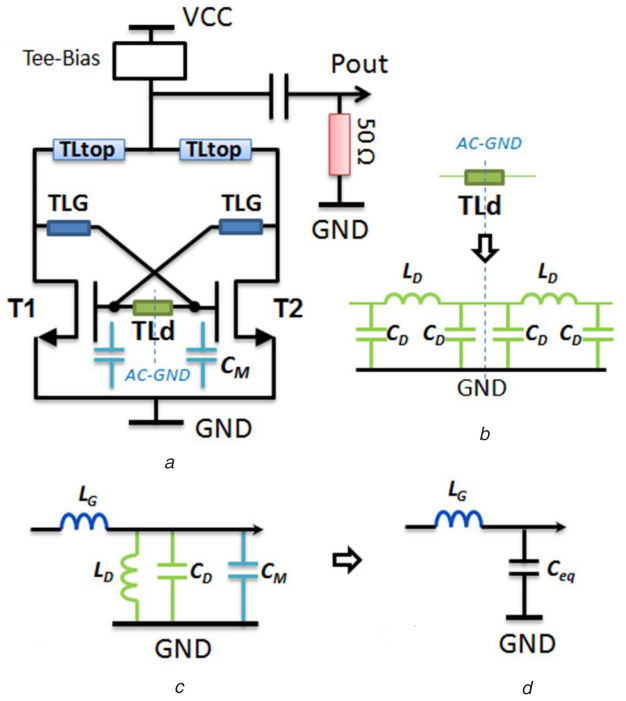


Fig. 3 *Oscillator design represented*
(a) Oscillator design with added TLd,
(b) Equivalent dual-section π-model for TLd assumed lossless,
(c) New delay cell with added elements L_D and C_D representing a half-length of TLd with respect to the middle AC-ground,
(d) Delay cell sketched with the equivalent capacitance C_{eq} of (L_D, C_D, C_M)

delay cell formed by (L_G, C_M). It can be demonstrated (analytically and by simulation) that the resulting oscillation frequency is given by

$$f_0 = \left(\frac{f_1}{a_1} // \frac{f_2}{a_2}\right) \tag{1}$$

where a_1 and a_2 are coefficients that can be related to the relative impedances of TLtop and the (L_G, C_M) delay cell, respectively, and f_1 and f_2 are the relative frequencies set by the delays through these TLs, such that

$$f_1 = \frac{1}{2}\frac{1}{2\pi\sqrt{L_G C_M}} \tag{2}$$

and

$$f_2 = \frac{1}{4}\frac{v}{2\pi l_{top}} \tag{3}$$

where l_{top} is the physical length of TLtop and v is the light velocity in the considered material.

In this paper, the introduced frequency enhancement effect is relative to the oscillation frequency increase through f_1. Thus, the following developments will be only in regard to this frequency. Note that the calculated frequency (2) does not take into account the equivalent capacitance at the MOS drain, which would even result in a lower fundamental frequency. As mentioned earlier, opting for longer TLG to present higher impedance or ideally an open circuit at the gate would also increase L_G and lower f_0. This behaviour defines a trade-off between maximising the output power and achieving a high oscillation frequency.

A similar design approach has been demonstrated in [9, 10, 14]. In [9], the gate blocking is applied on eight single-ended stages to extract the second harmonic through direct power combining. In [10], the gate blocking is employed in eight differential oscillators each generating the second harmonic along with radiated power combining. In [14], the gate-blocking impedance is used in a differential structure and connected in an oscillator loop of four cells. In this case, the fourth harmonic ($4f_0$) of the oscillation frequency is exploited to generate the output signal (quadruple push oscillator). In all these cases, having a large number of stages gives higher routing complexity, more parasitics, higher DC power consumption and an increasing chip area.

The proposed oscillator design is based on a differential structure to achieve compact form factor, simplified routing with less parasitics and reduced DC power consumption. A differential transmission line (TLd) is added between the cross-coupled transistor gates. Its equivalent series inductance (L_D) cancels part of the gate capacitance (C_M) in addition to the TLd's own distributed parasitic capacitance (C_D), as shown in Figs. 3*a* and *b*. This effect could be seen as a differential equalisation where by reducing the equivalent capacitance at the gate level, a higher oscillation frequency is obtained. Note that TLd has a negligible effect on the common mode behaviour as long as its own parasitic capacitance (C_D) can be made negligible compared to the equivalent gate capacitance (C_M).

The transmission line (TLd), assumed to be lossless, can be represented by a double section $C_D L_D C_D$ π-model, as depicted in Fig. 3*b*. The modified delay cell given in Fig. 3*c* includes L_D and C_D elements in parallel to C_M, and refers to a half-length of TLd with respect to the middle AC-ground. The parallel combination of L_D, C_D, and C_M is represented by an equivalent capacitance C_{eq} in the delay cell of Fig. 3*d*, such that

$$C_{eq} = C_M + C_D - \frac{1}{4\pi^2 f^2 L_D} \tag{4}$$

From (2), the new frequency (f'_1) could be written as

$$\begin{aligned} f'_1 &= \frac{1}{2}\frac{1}{2\pi\sqrt{L_G C_{eq}}} \\ &= \frac{1}{2}\frac{1}{2\pi\sqrt{L_G\left(C_M + C_D - (1/4\pi^2 f'^2_1 L_D)\right)}} \end{aligned} \tag{5}$$

Rearranging (5), we get

$$f'_1 = \sqrt{\frac{(1 + 4L_G/L_D)}{(1 + C_D/C_M)}} f_1 = \mathrm{FEF} \cdot f_1 \tag{6}$$

where f_1 is the initial frequency calculated in (2). From (6), it can be inferred that a FEF between f'_1 and f_1 has resulted from the proposed equalisation method. For a given TLG design, the MOST size, for a higher FEF would require lowering both L_D and C_D which leads to a relatively short TLd. Sizing TLd width is a compromise between several factors. For example, finding the minimum series resistance (giving wide TLd), maximising FEF, and setting the right characteristic impedance. Thus, an acceptable value for TLd could be determined through simulations.

To illustrate the potential of the proposed technique, Fig. 4 gives the evolution contours of FEF as a function of L_G/L_D and C_D/C_M ratios. As C_D can be considered negligible or lower than C_M, this lets us consider further the left side in Fig. 4. A large range of L_G/L_D settings can thus be chosen to easily obtain a FEF larger than one, and this is mainly due to the factor 4 in the numerator in (6). If we assume, for instance, that TLd has similar characteristics to the previously considered TLG ($L_G \simeq 15$ pH, $C_G \simeq 6$ fF), the resulting FEF gets roughly equal to two.

3 Implementation and modelling

The oscillator is implemented in a standard eight-metals 65 nm digital CMOS technology from ST Microelectronics. The top metal height is about only 5.7 µm from the substrate, which means that the parasitic capacitances (estimated to ~20 aF/µm^2 between M8 and M1) is quite high at the target frequency range. The oscillator design uses TL exclusively to avoid the power loss associated with

degraded quality factors of passive elements. Fig. 5*a* gives a descriptive schematic of the oscillator design and Fig. 5*b* shows a layer-level schematic illustrating TLG and TLd layout and connections to the MOSTs (T_1, T_2).

The modelling of the different oscillator circuit components is critical to accurately predict the oscillation frequency and the output power. This might be challenging as the routing of the MOSTs and TLs has many superposed layers and shared zones to isolate distributed and close mutual capacitances or inductances [19].

The MOSTs are sized to 40 µm width, 60 nm length and folded into 60 fingers. The substrate ring in M1 (part of the default library layout) is removed on one side and continued only with active (P+) layer to allow direct connection (with M1 and M2) from the gate to both TLG and TLd. This is done to achieve a minimum series resistance at the cost of slightly increased additional capacitance to the bulk. The source connection is made through parallel M2 and M3 layers to the circuit ground (GND) as shown in Fig. 5*b*. The capacitive parasitics due to the MOSTs' routing is extracted using

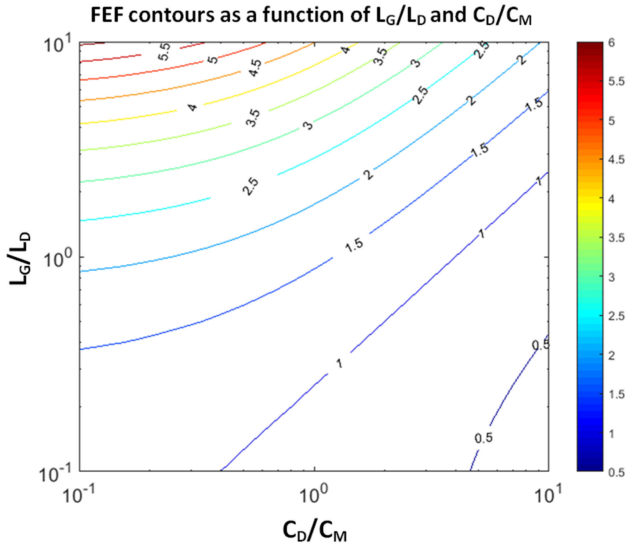


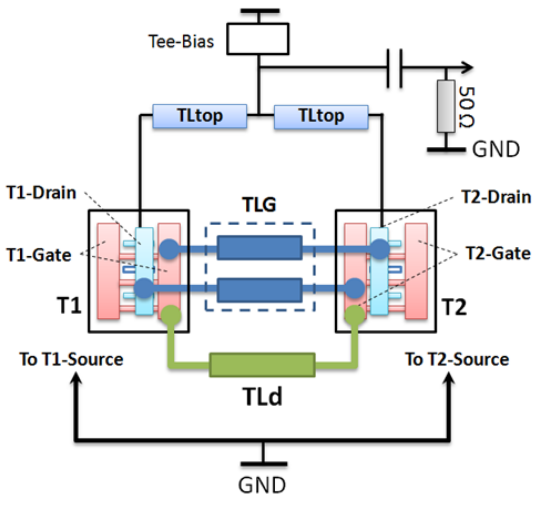
Fig. 4 *FEF contours as a function of of L_G/L_D and C_D/C_M ratios varied from 0.1 to 10 each*

Calibre software. The overlapping vias and metal-layer series resistance connected to either the drain or the source is simulated with Momentum software to take into account the resistance increase by the skin effect. The skin depth is estimated to be approximately 0.13 µm at 300 GHz. The extracted RC elements for each routed MOST are represented in Fig. 6*a*. To provide a minimum ohmic ground to the gm-core despite the very tight skin depth, two wide planes in M1 and M2 are connected over the complete circuit width (~ 200 µm) from the GND pads to the gm-core cell.

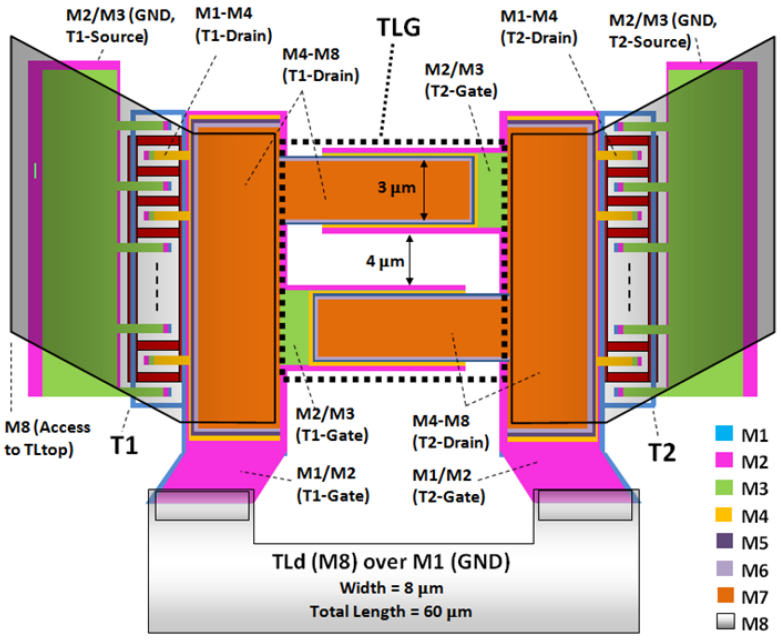
The TLG design is based on a compact and direct connection between the respective MOSTs drains and gates to minimise the inner spacing between transistors to around 7 µm. This avoids the CM power loss by asymmetrical connections caused by lines crossing. The spacing between both TLG microstrips is set to less than 4 µm and each trace is 3 µm wide (Fig. 5*b*). The TLG layout is made with stacked metals, i.e. a M2/M3 stack starting from the gate to reach the opposite drain with a M4/M7 stack to minimise the series losses with reduced traces dimensions and form factor. The lumped RLC model for the dual TLG lines is shown in Fig. 6*b*. This model is extracted using S-parameter curves fitting with a four-port Momentum layout. The model is split into dual sections for improved accuracy, with k_f representing the coupling factor between the respective line inductances [20].

The TLd is placed on the bottom side of the gm-core to provide a direct access to the MOS gates in M1/M2 layers as shown in Fig. 5*b*. The TL is laid out in M8 layer over M1 GND and sized to 60 µm total length and 8 µm width. The relative RLC model (see Fig. 6*c*) is extracted using S-parameter curves fitting with a two-port Momentum layout. The TLd line presents a characteristic impedance of 44 Ω.

While the RLC modelling helps define the initial design, EM simulation (done with Momentum) remains unavoidable to take into account the mutual capacitances and magnetic coupling between the different design components. The EM simulation should be extensive and includes all elements without compromising the meshing accuracy or increasing excessively the simulation time. In this design, EM simulations are done on two main parts: the *first* comprises the metal connections above the MOSTs, TLd, TLG, along with the surrounding ground plane as shown in Fig. 6*d*, and the *second* regards the top TLs (TLtop) connection to the ground–signal–ground measurement pads as shown in Fig. 7*a*.



a



b

Fig. 5 *Descriptive schematic of the oscillator design showing*
(a) TLd and TLG connections to the MOSTs,
(b) Layer-level layout of the different connections and TLs (scale not representative of the real dimensions)

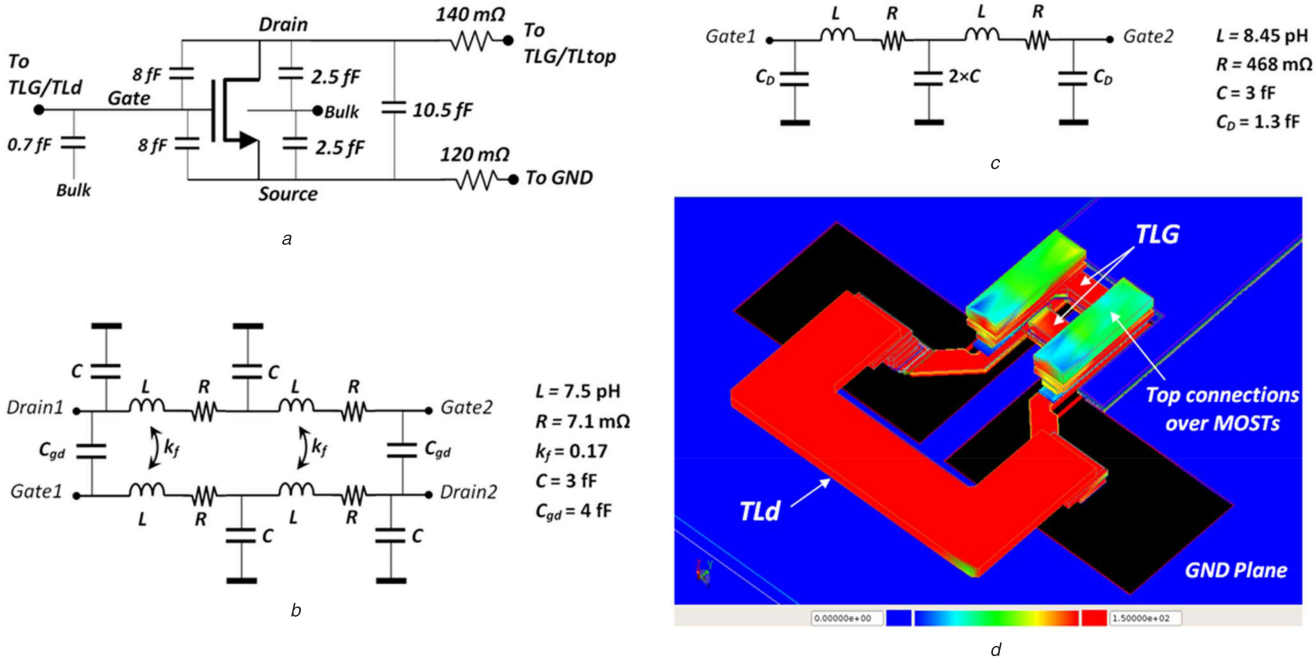


Fig. 6 *Extracted lumped RLC model*
(a) MOST routing,
(b) Dual-section model for TLG,
(c) TLd,
(d) EM-simulated Momentum layout including TLd, TLG, the top MOSTs' connections, and the surrounding GND plane

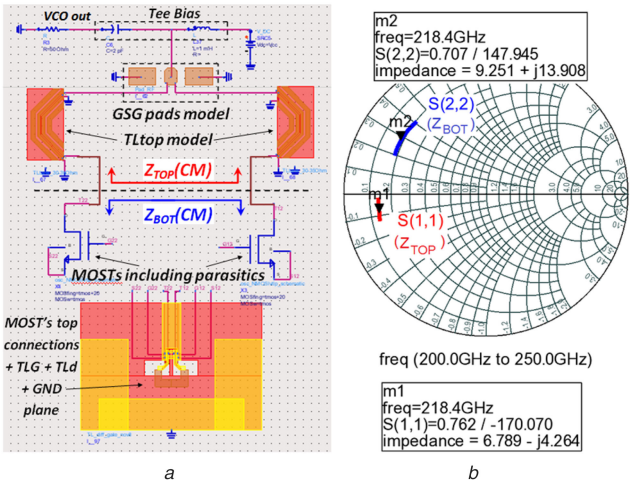


Fig. 7 *ADS simulation showing*
(a) The used schematic with the different EM-simulated-based models,
(b) Partial CM matching between the bottom oscillator impedance (Z_{BOT}) and the top part impedance (Z_{TOP}) at 218 GHz frequency

The TLtop model was included as two separate parts in the oscillator schematic (Fig. 7*a*) due to negligible mutual coupling between both lines with grounded sidewalls and bottom-M1 waveguide structure [21]. This also reduces the simulation time needed for optimisation due to the large layout area that would have taken a single EM-model for a dual TLtop layout. Each TLtop is sketched with a 12 µm wide M8 layer over 165 µm long track from the MOST to the signal pad. Shielding sidewalls are formed with M8-to-M1 metal stack and set to 13 µm width and 6 µm spacing away from the signal track. The TL gives around 40 Ω characteristic impedance.

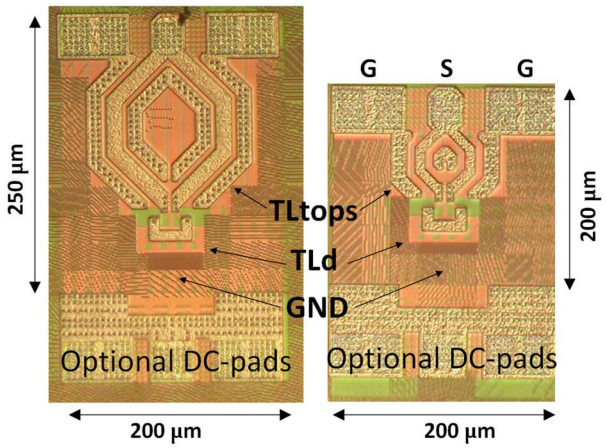
Starting with $\lambda/2$ length at $2f_0$ for TLtop lines provides 50-Ω CM impedance for Z_{TOP} (looking upwards in Fig. 7*a*). With an inductive CM impedance presented by the entire bottom part of the oscillator (Z_{BOT} in Fig. 7*b*), a matching issue comes up with a non-optimum CM power transfer situation. A solution would consist of shortening TLtop length to allow Z_{TOP} rotation on the Smith chart (see Fig. 7*b*) in order to place it on the conjugate side of Z_{BOT} for optimum CM matching. The counterpart of this design change is the partial contribution of TLtop to the oscillation frequency (f_0) by creating a parallel differential path to the gm-core's one. Managing both constraints in terms of CM impedance matching and oscillation frequency sets TLtop length to slightly less than $\lambda/4$ (or ∼165 µm) for a final simulated frequency at 218 GHz and −6.1 dBm output power under 1.5 V DC supply voltage. The partial CM matching in this case is shown in Fig. 7*b*. This oscillator version is termed (OSC1). Another version (OSC2) of this oscillator design has a shortened TLtop length of 70 µm to assess the effect on the frequency shift. TLtop is modified without any matching optimisation effort and with an expected power performance penalty. The simulated oscillation frequency for OSC2 showed around 250 GHz with about −9 dBm output power from 1.5 V DC supply voltage. The main goal of this VCO design is to illustrate the fundamental frequency enhancement effect while targeting a very small layout form factor. Additional effort is needed to increase the output power via on-chip or spatial combining.

4 Measurement results

Micrographs of the implemented oscillators OSC1 and OSC2 are shown in Figs. 8*a* and *b*, respectively. Both oscillators were directly probed on chip. The effective area is 200 µm × 250 µm and 200 µm × 200 µm for OCS1 and OSC2, respectively.

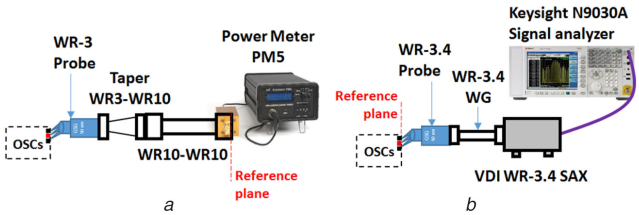
The testing setups are given in Figs. 9*a* and *b* for power and frequency measurements, respectively. Erickson PM5 power meter from Virginia Diodes Inc. (VDI) was used for power measurements, while VDI WR-3.4 SAX down-converter in addition to Keysight N9030A signal analyser was employed for frequency and phase-noise measurements. Both oscillators were tested in free-running mode without any frequency locking.

Measured oscillation frequencies for both oscillators showed an upward shift compared to simulations. OSC1 has an oscillation frequency from 248 to 251 GHz for a supply voltage (VDD) varied from 1.2 to 1.5 V as shown in Fig. 10*a*. This is compared to 218 GHz from simulations. The deviation in frequency can be due to conservative modelling (mainly with the MOST parasitics) and to the difficulty of separating shared or overlapping connections as well as too close mutual capacitances or magnetic coupling that would have been accounted multiple times. OSC2 presents about



a b

Fig. 8 *Implemented oscillator micrographs*
(a) OSC1,
(b) OSC2



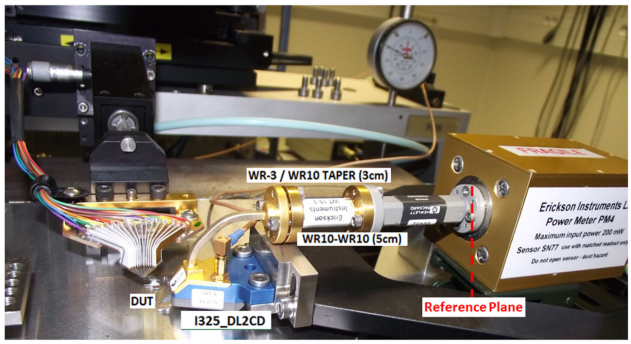
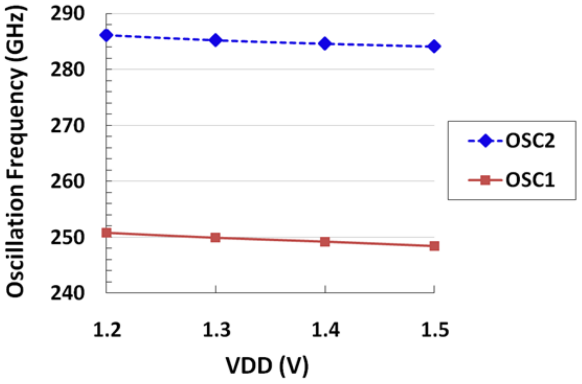


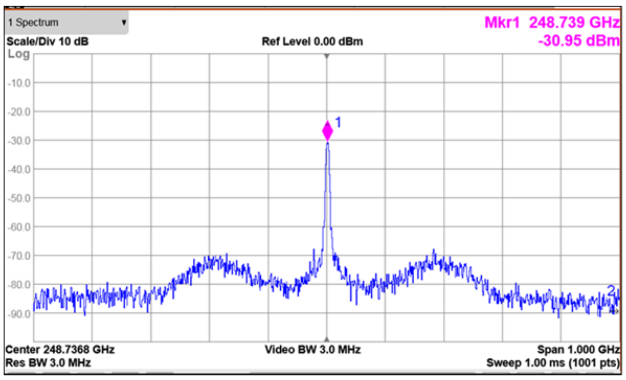
Fig. 9 *Testing setups*
(a) Power,
(b) Frequency measurement,
(c) Real (power) setup

0.7% frequency tuning range versus VDD with a ranging frequency from 284 to 286 GHz. Single-tone measurements at VDD = 1.5 V are given in Figs. 10*b* and *c* for OCS1 and OSC2, respectively.

Power measurements are corrected with the different setup losses summarised in Table 1. The resulting output power figures after losses extraction are depicted for both oscillators in Figs. 11*a* and *b* as a function of VDD. OSC1 maximum output power reached −8.1 dBm at VDD = 1.5 V. OSC2 showed −14.8 dBm output power under 1.5 V. DC power consumptions for both oscillators versus VDD are also given in Figs. 11*a* and *b* with maximum 76 and 80 mW for OSC1 and OSC2, respectively. Output power deviations between simulated and measured results could also be explained by the MOST modelling as part of the combined wires resistance was based on extrapolating the Calibre-found resistance to include the skin effect. Other reasons could be due to some over or under estimated shared connections or inter-metal layers vias or deviation from transistor parameters post-fabrication.

Phase noise measurements are carried out using the same measurement setup with the N9030A signal analyser. OSC1 gives at 10 MHz offset around −104 dBc/Hz and −106.8 dBc/Hz under 1.2 and 1.5 V supply voltage, respectively. OSC2's phase noise is





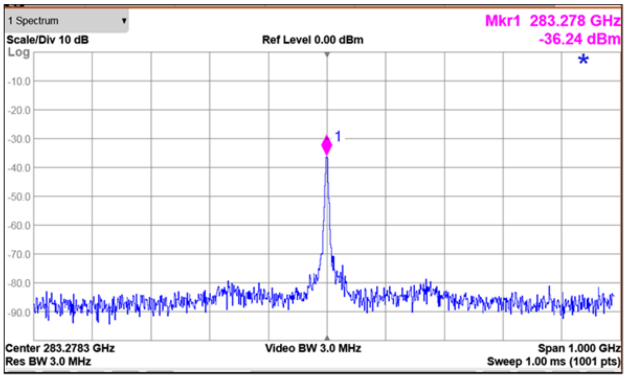


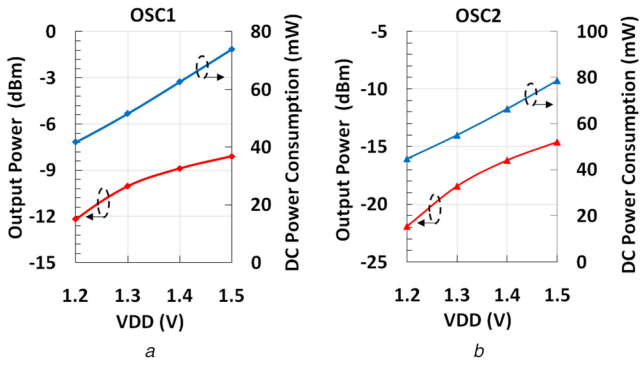
Fig. 10 *Measured oscillation frequency*
(a) Versus VDD for both oscillators,
(b) OSC1 at VDD = 1.5 V,
(c) OSC2 at VDD = 1.5 V

Table 1 Setup power losses (in dB)

Circuit	Pad	I325_DL2CD (probe)	WR3/WR10 taper (3 cm)	WR10 WG (5 cm)
OSC1 (250 GHz)	0.5	3.0	0.35	0.375
OSC2 (285 GHz)	0.5	3.4	0.385	0.39

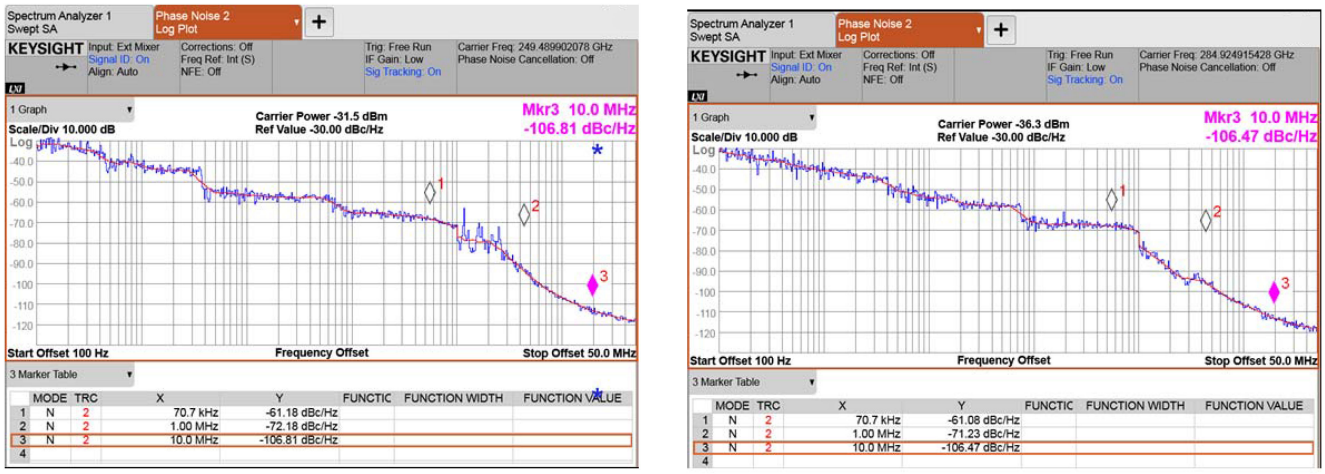
around −106 dBc/Hz at 10 MHz offset for both 1.2 and 1.5 V VDD. Measured phase noise curves for OSC1 and OSC2 at VDD = 1.5 V are given in Figs. 12*a* and *b*, respectively. A plateau is present up to a few MHz offset due to the unlocked oscillation frequency. A slope between −30 and −20 dB/decade starts appearing from 10 MHz offset.

This work is compared with the state of the art of THz oscillators implemented in 65-nm CMOS technology in the 250–300 GHz range in Table 2. The presented single-stage oscillators in our case can be distinguished by the low DC power consumption but also by the lowest form factor. The proposed architecture can



a *b*

Fig. 11 *Measured output power (after losses extraction) and DC power consumption versus VDD*
(a) OSC1,
(b) OSC2



a *b*

Fig. 12 *Measured phase noise at VDD = 1.5 V*
(a) OSC1,
(b) OSC2

Table 2 Published 250–300 GHz VCOs in 65-nm CMOS

Ref.	Freq., GHz	P_{out}, dBm	P_{DC}, mW	Phase noise, dBc/Hz	Area, μm × μm
[7][a]	239	−4.8	18.5	−98.43 to −110.9 @ 10 MHz	400 × 450
[9][b]	256	4.1	227	−94 @ 1 MHz	670 × 650
[10][c]	260	0.5	800	−78.3 @ 1 MHz	1500 × 1500
[11][d]	288	−1.5	275	−87 @ 1 MHz	500 × 570
[13][e]	298	0.9	235	−79 @ 1 MHz	290 × 316
[14][f]	290	−1.2	325	−78 @ 1 MHz	600 × 600
this work (OSC1)	248	−9	76	−106.8 @ 10 MHz	200 × 250
this work (OSC2)	284	−15	80	−106.47 @ 10 MHz	200 × 200

[a]Single transformer-based push–push ($2f_0$) VCO.

[b]Eight single-ended second-harmonic ($2f_0$) VCOs.

[c]Eight coupled differential self-feeding second-harmonic ($2f_0$) VCOs.

[d]Two mutually coupled single-ended triple-push ($3f_0$) oscillator cores.

[e]Quad-core-coupled triple-push ($3f_0$) VCOs.

[f]Four coupled differential fourth-harmonic ($4f_0$) VCOs.

be evolved into a coupled-array source to increase the output power while keeping a low DC-power level as well as a small form factor advantage. This is an essential characteristic for large-scale THz systems integration in low-cost CMOS processes.

5 Conclusion

In this paper, a push–push oscillator architecture based on differential gate equalisation to enhance the oscillation frequency while achieving an ultra-compact design form factor has been presented. The frequency enhancement is derived as a function of the equivalent RLC components of the oscillator's design parts. The design concept has been proven on two single-stage push–push oscillators implemented in standard digital 65-nm CMOS technology. Measured oscillation frequencies showed around 250 and 285 GHz with output power levels around −8.1 and −14.8 dBm, respectively. Phase noise levels are at −106.8 and −106 dBc/Hz at 10 MHz offset. The achieved design area below 200 × 250 μm^2 represents a key feature for potential large-scale integrated coupled-oscillator arrays in low-cost and digital CMOS technologies.

6 Acknowledgment

The authors would like to thank Keysight for assistance with testing.

7 References

[1] Nagatsuma, T.: 'THz communication systems'. Optical Fiber Communication Conf. (OFC), OSA Technical Digest, paper Tu3B.1, March 2017

[2] Park, K.H., Lee, E.S., Lee, I.-M., *et al.*: 'Semiconductor-based terahertz photonics for industrial applications'. Optical Fiber Communication Conf. (OFC), OSA Technical Digest, paper W4B.4, March 2017

[3] Muralidharan, S., Wu, K., Hella, M.: 'A 165–230 GHz SiGe amplifier-doubler chain with 5 dBm peak output power'. IEEE Radio Frequency Integrated Circuits Symp., 2016

[4] Wu, K., Muralidharan, S., Hella, M.: 'A wideband SiGe BiCMOS frequency doubler with 6.5-dBm peak output power for millimeter-wave signal sources', *IEEE Trans. Microw. Theory Tech.*, 2018, **66**, (1), pp. 187–200

[5] Ergintav, A., Ng, H.J.: 'An integrated 240 GHz differential frequency sixtupler in SiGe BiCMOS technology'. 17th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), 2017

[6] Lin, H.-C., Rebeiz, G.M.: 'A 200–245 GHz balanced frequency doubler with peak output power of +2 dBm'. IEEE Compound Semiconductor Integrated Circuit Symp. (CSICS), 2013

[7] Koo, H., Hong, S.: 'Design and analysis of 239 GHz CMOS push-push transformer-based VCO with high efficiency and wide tuning range', *IEEE Trans. Circuits Syst. I, Regul. Pap.*, 2015, **62**, (7), pp. 1883–1893

[8] Kananizadeh, R., Momeni, O.: 'High-power and high-efficiency millimeter-wave harmonic oscillator design exploiting harmonic positive feedback in CMOS', *IEEE Trans. Microw. Theory Tech.*, 2017, **65**, (10), pp. 3922–3936

[9] Adnan, M., Afshari, E.: 'A 247-to-263.5 GHz VCO with 2.6 mW peak output power and 1.14% DC-to-RF efficiency in 65 nm bulk CMOS'. IEEE Int. Solid-State Circuits Conf. Digest of Technical Papers (ISSCC), 2014, pp. 262–263

[10] Han, R., Afshari, E.: 'A CMOS high-power broadband 260-GHz radiator array for spectroscopy', *IEEE J. Solid-State Circuits*, 2013, **48**, (12), pp. 3090–3104

[11] Grzyb, J., Zhao, Y., Pfeiffer, U.R.: 'A 288-GHz lens-integrated balanced triple-push source in a 65-nm CMOS technology', *IEEE J. Solid-State Circuits*, 2013, **48**, (7), pp. 1751–1761

[12] Momeni, O., Afshari, E.: 'High power terahertz and millimeter wave oscillator design: a systematic approach', *IEEE J. Solid-State Circuits*, 2011, **46**, (3), pp. 583–597

[13] Tousi, Y.M., Momeni, O., Afshari, E.: 'A 283-to-296 GHz VCO with 0.76 mW peak output power in 65 nm CMOS'. IEEE Int. Solid-State Circuits Conf. Digest of Technical Papers (ISSCC), 2012, pp. 258–260

[14] Shirazi, A.H.M., Nikpaik, A., Mirabbasi, S., *et al.*: 'A quadcore-coupled triple-push 295-to-301 GHz source with 1.25 mW peak output power in 65 nm CMOS using slow-wave effect'. IEEE Radio Frequency Integrated Circuits Symp. (RFIC), 2016, pp. 190–193

[15] Jameson, S., Halpern, E., Socher, E.: 'A 300 GHz wirelessly locked 2×3 array radiating 5.4 dBm with 5.1% DC-to-RF efficiency in 65 nm CMOS'. IEEE Int. Solid-State Circuits Conf. (ISSCC) Digest of Technical Papers, 2016, pp. 348–349

[16] Muralidharan, S., Wu, K., Hella, M.: 'A 110–132 GHz VCO with 1.5 dBm peak output power and 18.2% tuning range in 130 nm SiGe BiCMOS for D-band transmitters'. 2016 IEEE 16th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), Austin, TX, 2016, pp. 64–66

[17] Nikpaik, A., Masnadi Shirazi, A.H., Nabavi, A., *et al.*: 'A 219-to-231 GHz frequency-multiplier-based VCO with ∼3% peak DC-to-RF efficiency in 65-nm CMOS', *IEEE J. Solid-State Circuits*, 2018, **53**, (2), pp. 389–403

[18] Wu, K., Hella, M.: 'A 103-GHz voltage controlled oscillator with 28% tuning range and 4.2 dBm peak output power using SiGe BiCMOS technology'. 2018 IEEE/MTT-S Int. Microwave Symp. – IMS, Philadelphia, PA, 2018, pp. 606–609

[19] Beattie, M., Pileggi, L.: 'On-chip induction modeling: basics and advanced methods', *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, 2002, **10**, (6), pp. 712–729

[20] Kopcsay, G.V., Krauter, B., Widiger, D., *et al.*: 'A comprehensive 2-D inductance modeling approach for VLSI interconnects: frequency-dependent extraction and compact circuit model synthesis', *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, 2002, **10**, (12), pp. 665–711

[21] Elgamel, M., Kumar, A., Bayoumi, M.: 'Efficient shield insertion for inductive noise reduction in nanometer technologies', *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, 2005, **13**, (3), pp. 401–405